

AMENDMENTS TO THE CLAIMS:**Listing of Claims:**

This listing of claims will replace all prior versions, and listings, of claims in the application:

CLAIMS 1-5 (Canceled).

CLAIM 6 (Canceled).

7. (Currently Amended) An IC tag for transmitting first information to a reception unit, comprising:

- a ~~first~~ memory which memorizes the first information and a ~~second~~ memory which ~~memorizes~~ second information; and
- a counter in which its count value indicates a bit address of the ~~first~~ memory, wherein the IC tag carries out count-up or count-down of a count value of the counter according to a clock signal received from the reception unit and the IC tag sets the second information of ~~the second memory~~ as an initial value of the counter and after the count value of the counter reaches a specified code, the first information stored in the bit address of ~~the first memory~~ indicated by the count value is sent out to the reception unit successively.

8. (Currently Amended) The IC tag according to claim 7,

- wherein the ~~second memories~~ are provided in plural number memory memorizes the third information and the IC tag sets either the second information of ~~any one of the second memories~~ or the third information as an initial value of the counter.

9. (Currently Amended) The IC tag according to claim 8, further comprising a mode switching portion,

wherein the IC tag selects ~~the second information of any one of the second memories~~ the second information or the third information by means of the mode switching portion and sets it as an initial value of the counter.

10. (Currently Amended) The IC tag according to claim 9,

wherein the mode switching portion is a flip-flop and the IC tag selects the ~~second information of any one of the second memories~~ the second information or the third information according to a value of the flip-flop and sets it as an initial value of the counter.

11. (Original) The IC tag according to claim 10,

wherein the specified code is zero.

12. (Currently Amended) The IC tag according to claim 10,

wherein the counter and ~~the second memory~~ the second information have the same bit number.

13. (Currently Amended) The IC tag according to claim 10,

wherein the first information is comprised of at least an identification number and an error detection code for detecting an error in the identification number.

14. (Currently Amended) A reading method for reading ~~the first information~~ from an IC tag having a ~~first~~ memory which memorizes first information, ~~a second~~

~~memory which memorizes and second information and a counter in which a count value thereof indicates a bit address of the first memory to the reception unit,~~
comprising:

transmitting a clock signal from the reception unit to the IC tag;

setting the second information of the second memory in the IC tag as an initial value of the counter;

performing count-up or count-down of a count value of the counter according to the clock signal; and

after the count value of the counter reaches a specified code, transmitting the first information stored in the bit address of the first memory indicated with the count value successively to the reception unit.

15. (Currently Amended) The reading method according to claim 14,
wherein the ~~second memories of the IC tag are provided in plural number~~
memory memorizes the third information and the second information of any one of
the ~~second memories~~ is selected according to the mode switching signal and set up in the IC tag as an initial value of the counter.

16. (Original) The IC tag according to claim 8,
wherein the specified code is zero.

17. (Original) The IC tag according to claim 9,
wherein the specified code is zero.

18. (Currently Amended) ~~The IC tag according to claim 10,~~ The reading method according to claim 14,

wherein the specified code is zero.

19. (Original) The IC tag according to claim 8,
wherein the counter and the second memory have the same bit number.

20. (Original) The IC tag according to claim 9,
wherein the counter and the second memory have the same bit number.

21. (Currently Amended) ~~The IC tag according to claim 10,~~ The reading method according to claim 14,

wherein the counter and the second memory have the same bit number.

22. (Currently Amended) The IC tag according to claim 8,
wherein the first information is comprised of at least an identification number
and an error detection code for detecting an error in the identification number; and
wherein the second information is a random number.

23. (Currently Amended) The IC tag according to claim 9,
wherein the first information is comprised of at least an identification number
and an error detection code for detecting an error in the identification number.

24. (Currently Amended) ~~The IC tag according to claim 10,~~ The reading method according to claim 14,

wherein the first information is comprised of at least an identification number
and an error detection code for detecting an error in the identification number; and
wherein the second information is a random number.